150 DEGREE BUMP PLACEMENT LAYOUT FOR AN INTEGRATED CIRCUIT POWER GRID

Abstract

A 150 degree bump placement layout for an integrated circuit power grid is provided. This layout improves integrated circuit performance and reliability and gives an integrated circuit designer added flexibility and uniformity in designing the integrated circuit. Further, a patterned bump array for a top metal layer of an integrated circuit having a plurality of 150 degree bump placement structures is provided.

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